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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/925,889	08/06/2001	Rasekh Rifaat	A0312/7412 WRM/IB	6192

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EXAMINER	
BURD, KEVIN MICHAEL	
ART UNIT	**PAPER NUMBER**
2611	

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/925,889	RIFAAT ET AL.	
	Examiner	Art Unit	
	Kevin M. Burd	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 16-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 16-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. This office action, in response to the remarks and declaration filed after final, is a non-final office action.

Response to Arguments

2. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

3. Applicant's arguments with respect to the rejections of the pending claim have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground of rejection is made in view of Lee (EP 1 017 183 A2).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-14 and 16-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee (EP 1 017 183 A2).

Regarding claims 1 and 8, Lee discloses a method for the despreading of spread spectrum signals in a digital signal processor. The process is performed in response to the generation to the single instruction by placing in the data path a DSP process that will perform the despreading operation by performing various multiplications,

summations and accumulations, all in a single instruction cycle (abstract). The despreading operation of the spread spectrum RAKE receiver consists of a process involving multiply-and-accumulate (MAC) operations for complex valued quantities (paragraph 0007).

Regarding claims 2 and 9, the method further includes including a previous result from a previous instruction in the complex addition which provides the despread result (paragraph 0009).

Regarding claims 3 and 10, the spreading factor is disclosed in paragraph 0005.

Regarding claims 4, 5, 11 and 12, the PN sequence is a sequence of +1 and –1 for the I and Q components (paragraph 0007).

Regarding claims 6, 7, 13 and 14, the incoming signal is stored in buffers of size N. the signal comprises real and imaginary bits (paragraph 0016).

Regarding claim 16, Lee discloses a digital signal processor shown in figure 1. The processor includes a memory 322, instruction generator 316, in path processor block 310 and numerous process blocks 320. The digital signal processor executes a method for the despreading of spread spectrum signals in a digital signal processor. The process is performed in response to the generation to the single instruction by placing in the data path a DSP process that will perform the despreading operation by performing various multiplications, summations and accumulations, all in a single instruction cycle (abstract). The despreading operation of the spread spectrum RAKE receiver consists of a process involving multiply-and-accumulate (MAC) operations for complex valued quantities (paragraph 0007).

Regarding claim 17, the spreading factor is disclosed in paragraph 0005.

Regarding claims 18 and 19, the PN sequence is a sequence of +1 and –1 for the I and Q components (paragraph 0007).

Regarding claims 20 and 21, the incoming signal is stored in buffers of size N. the signal comprises real and imaginary bits (paragraph 0016).

Regarding claim 22, Lee discloses a method for calculating output data in a digital signal processor. The process is performed in response to the generation to the single instruction by placing in the data path a DSP process that will perform the despreading operation by performing various multiplications, summations and accumulations, all in a single instruction cycle (abstract). The operation of the DSP consists of a process involving multiply-and-accumulate (MAC) operations for complex valued quantities (paragraph 0007).

Regarding claim 23, the PN sequence is a sequence of +1 and –1 for the I and Q components (paragraph 0007).

Regarding claims 24 and 25, the method despreads an incoming signal (abstract).

Regarding claim 26, the received signal is a spread spectrum/CDMA signal (abstract).

Regarding claim 27, Lee discloses a method for calculating output data in a digital signal processor. The process is performed in response to the generation to the single instruction by placing in the data path a DSP process that will perform the despreading operation by performing multiplication in a single instruction cycle

(abstract). The operation of the DSP consists of a process involving multiply-and-accumulate (MAC) operations for complex valued quantities (paragraph 0007).

Regarding claim 28, Lee discloses a method for calculating output data in a digital signal processor. The process is performed in response to the generation to the single instruction by placing in the data path a DSP process that will perform the despreading operation by performing various multiplications, summations and accumulations, all in a single instruction cycle (abstract). The operation of the DSP consists of a process involving multiply-and-accumulate (MAC) operations for complex valued quantities (paragraph 0007).

Regarding claim 29, the incoming signal is stored in buffers of size N. the signal comprises real and imaginary bits (paragraph 0016).

Regarding claim 30, the PN sequence is a sequence of +1 and –1 for the I and Q components (paragraph 0007).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Peleg et al (US 6,035,316) discloses in response to a single instruction (column 5, lines 25-30), complex multiplication and addition is carried out in a single clock cycle (column 22, lines 1-14). The processed data is then stored (column 3, line 63 to column 4, line 22). Takewa et al (US 6,092,183) discloses calculating an output signal in response to a single instruction, performing complex multiplication in a single clock cycle (figure 2a). Pechanek et al (US 7,072,929) discloses an apparatus for

the single cycle computation comprising multiplier means, adder means and storage means (column 11, line 62 to column 12, line 39).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin M. Burd whose telephone number is (571) 272-3008. The examiner can normally be reached on Monday - Friday 9 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Kevin M. Burd
9/4/2006

KEVIN BURD
PRIMARY EXAMINER